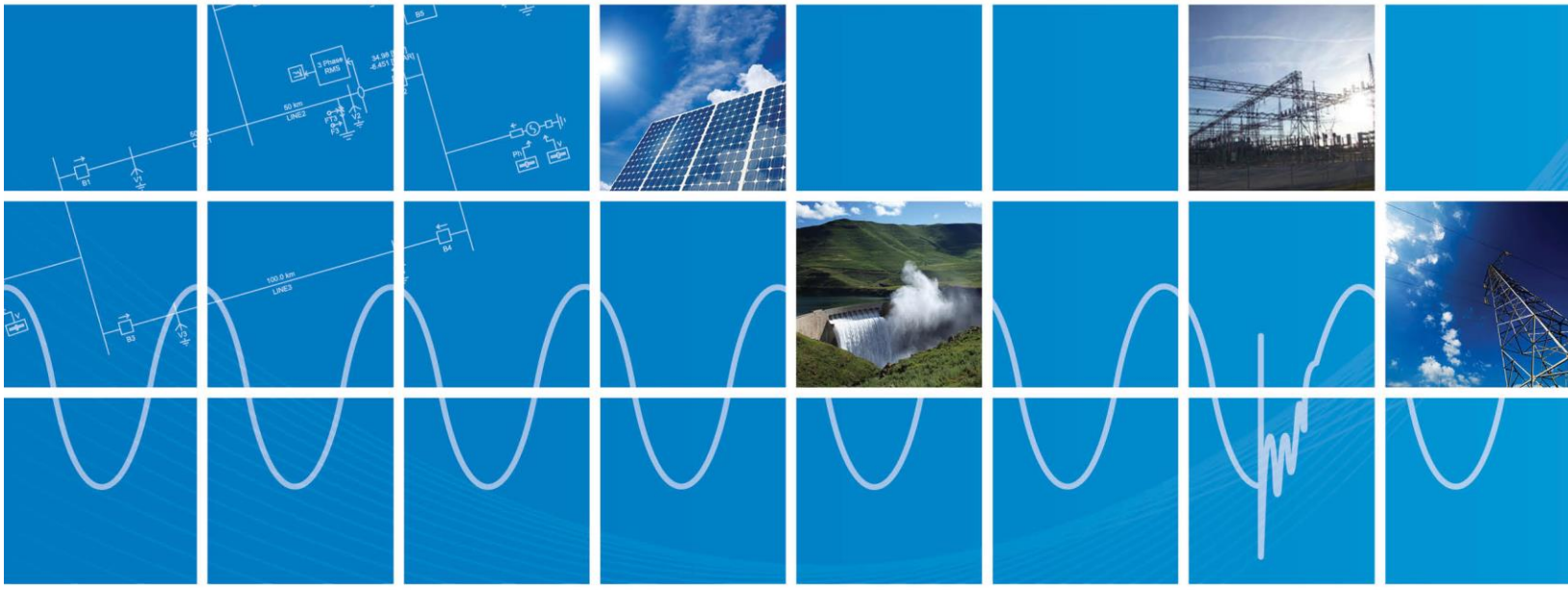
Phase Locked Loop (PLL) Component

For PSCAD Version 5.0

January 30, 2020

Initial



Powered by Manitoba Hydro International Ltd.
211 Commerce Drive
Winnipeg, Manitoba
R3P 1A3 Canada
mhi.ca

Manitoba HYDRO INTERNATIONAL

CONTENTS

1. OVERVIEW

Figure 1 illustrates the block diagram of the phase locked loop. Va, Vb and Vc are per-unitized instantaneous voltage of a three phase electrical system. G_p and G_I are the proportional gain and integral gain of the phase locked loop. The Park transformation is expressed in matrix form in equation (1). Function $\tan^{-1}\left(\frac{V_q}{V_d}\right)$ returns the phase angle of the complex number $V_d + jV_q$.

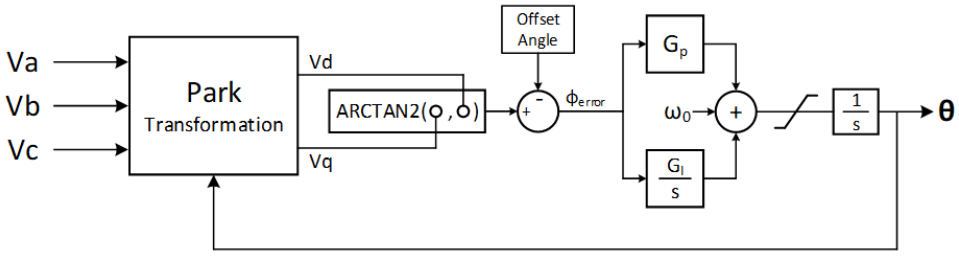


Figure 1: Block Diagram of PLL

$$\begin{bmatrix} V_q \\ V_d \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ sin(\theta) & sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

2. PSCAD/EMTDC EXAMPLE DESCRIPTION

2.1. Example 1:

The purpose of this example is to demonstrate how PSCAD/EMTDC PLL component performs. An open loop PLL was developed using master library component to benchmark against PSCAD/EMTDC Master library PLL component as shown in Figure 2. The settings for the master library PLL and the open loop PLL model are set to be identical.

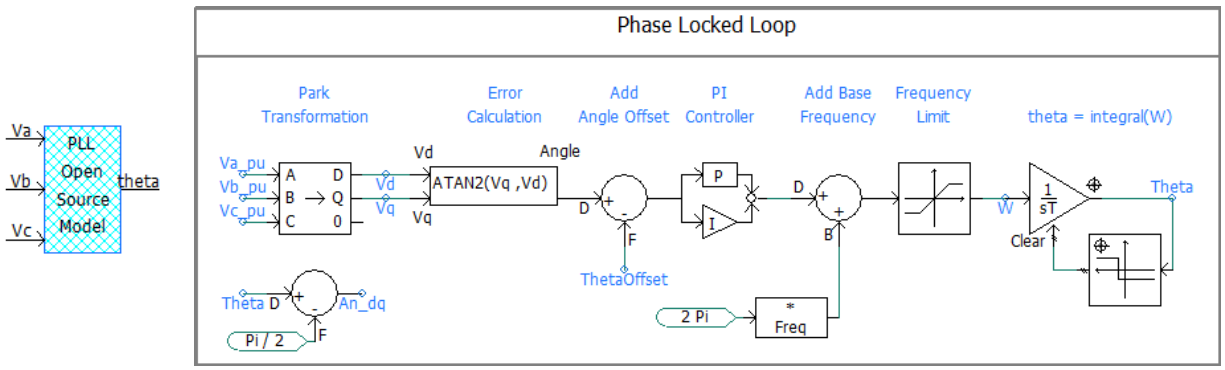


Figure 2: Phase Locked Loop Open Source Model

Figure 3a generates "Theta_Ref" and was used to demonstrate the response of PLL to the following scenarios,

- Increase the source phase angle by 90° (Figure 3b)
- Increase the source frequency from 60 Hz to 65 Hz in a rate of 100Hz/s (Figure 3b)

(a)

(b)

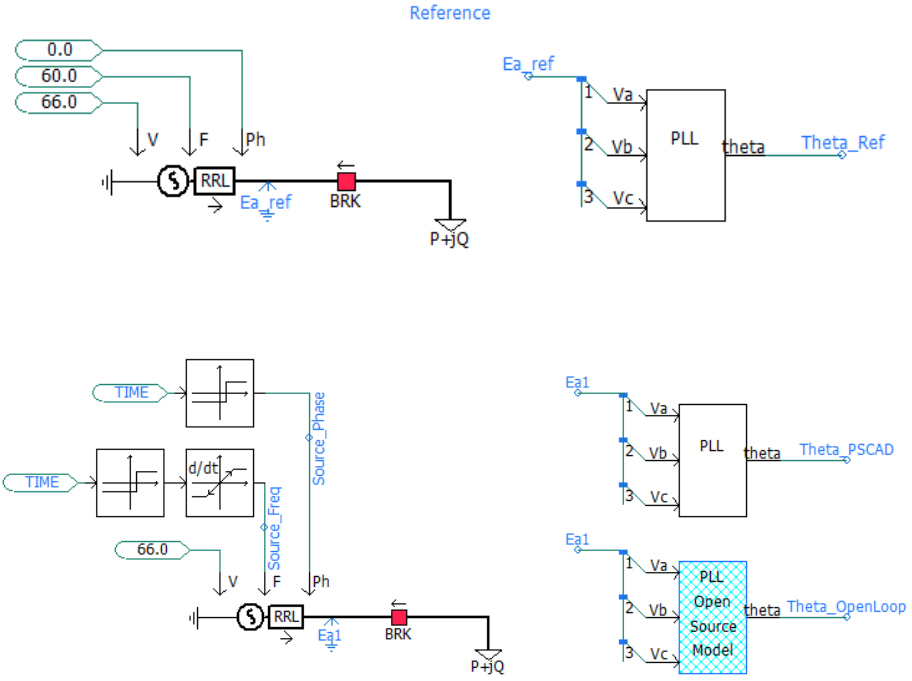


Figure 3: Case (a) was created to generate Theta_Ref to illustrate the PLL responses to different disturbances in case (b)

Figure 4 and Figure 5 compare the response of both PLL models. As expected, the open loop model matches the PLL component from PSCAD/EMTDC master library.

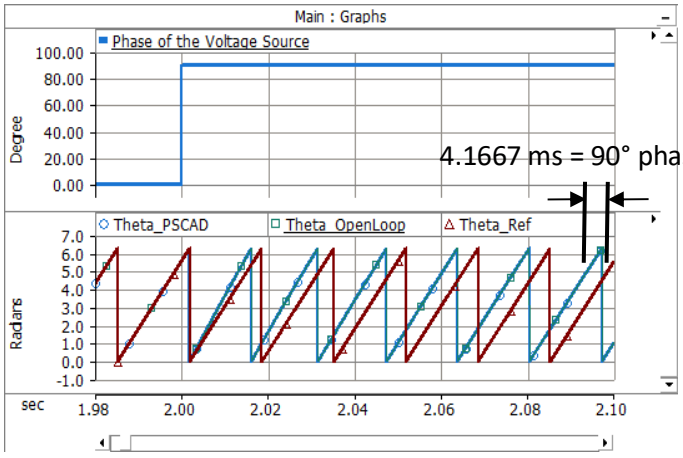


Figure 4: Phase of the Voltage Source and the PLL Phase Output

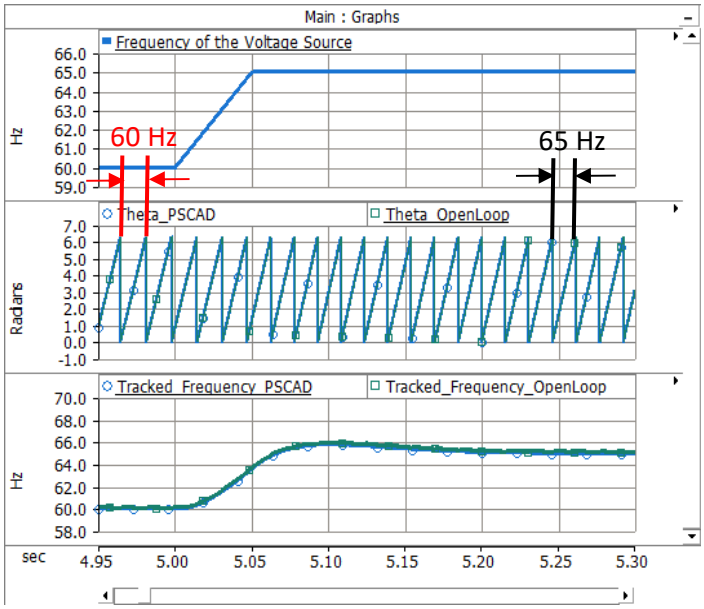


Figure 5: Comparison between the PSCAD Master Library PLL Model and the Open Source PLL Model

2.2. Example 2:

The purpose of this example is to demonstrate the performance of PSCAD/EMTDC PLL component under load rejection. Figure 6 shows the network configuration before and after load rejection. The phase and frequency of the voltage at the terminal of the equivalent source are tracked by the PLL as depicted in Figure 7. The phase shift between Theta_Ref and Theta is due to load rejection.

(a)

(b)

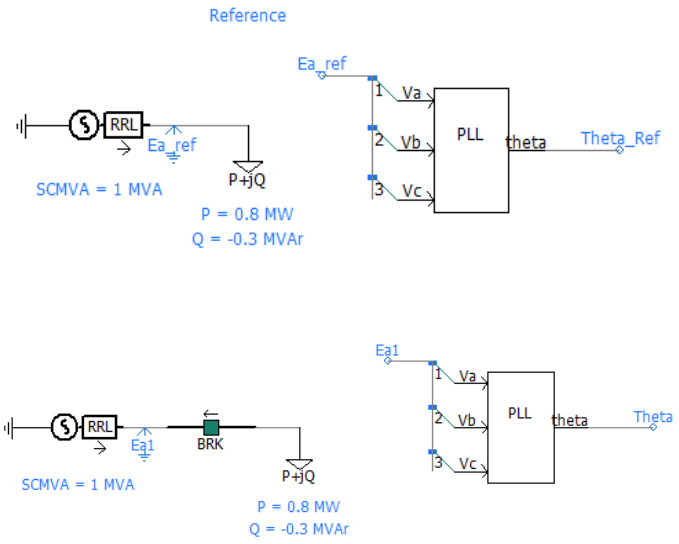


Figure 6: Network Configuration (a) before load rejection (b) after load rejection

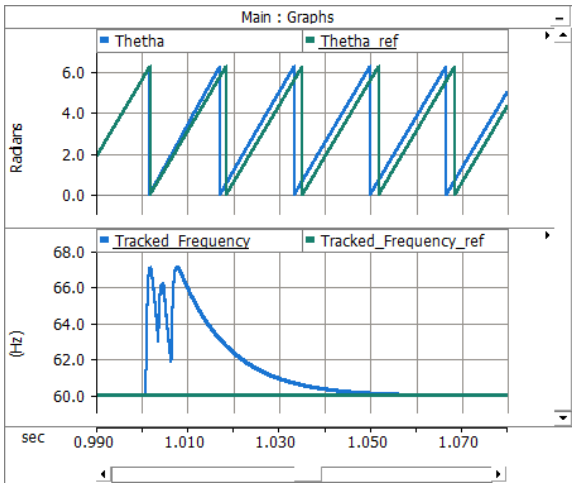


Figure 7: PLL Phase Output and Tracked Frequency

2.3. Example 3:

The purpose of this example is to demonstrate the impact of PLL control parameters (the proportional gain (Kp) and integral gain (Ki)) on its response. Table 1 summarizes the PLL control parameters for each test case.

Table 1: PLL Models Parameter Comparison

Parameters	PLL Model 1	PLL Model 2
Kp	300	30
Ki	1000	3000

Figure 8 shows a simple example where an equivalent source is connected to a 15 MW load through a 20 km transmission line. A solid 1-phase to ground fault was applied at the load side at 0.5s. The fault was cleared by opening of the breaker at 0.6s to isolate the fault from the system.

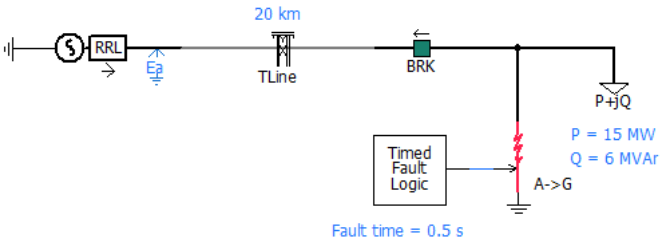


Figure 8: Network Configuration

Figure 9 compares the PLL response with different control parameters (Table 1). The PLL with larger integral gain shows better frequency response during the fault. The 120 Hz oscillation was caused by the negative sequence component of the network during the fault.

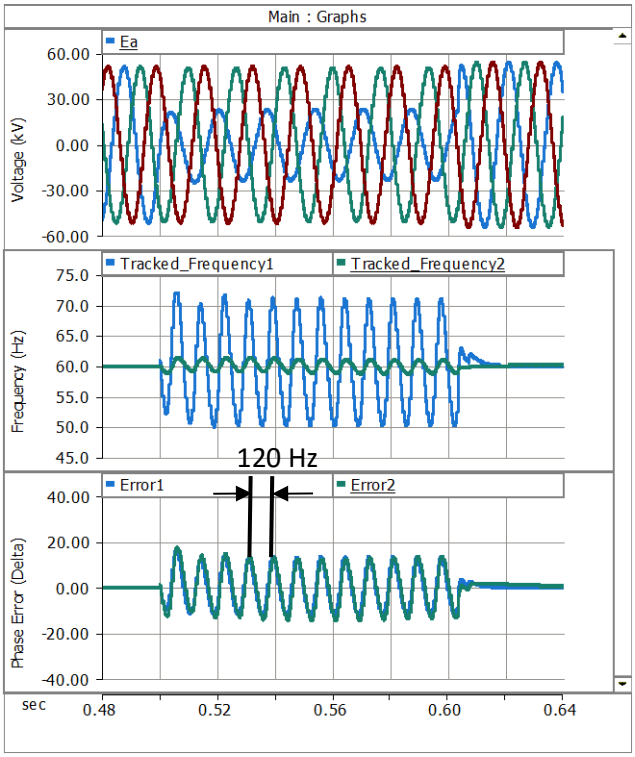


Figure 9: Measured Voltage, Tracked Frequency and Phase Error

DOCUMENT TRACKING

Rev.	Description	Date
0	Initial	30/Jan/2020